WHAT IS CLAIMED IS:

1. A liquid crystal display comprising:

a liquid crystal panel including a gate line, a data line, and a pixel including a switching element connected to the gate line and the data line;

a gate driver applying a gate signal for controlling the switching element to the gate line; and

a data driver selecting gray voltages corresponding to gray signals and applying the selected gray voltages to the data line,

wherein the gate signal includes a gate-on voltage for turning on the switching element and a gate-off voltage for turning off the switching element and the gate-on voltage has at least two different levels.

2. The liquid crystal display of claim 1, wherein the gate-on voltage continuously varies for a predetermined time.

3. The liquid crystal display of claim 2, wherein the at least two level includes a first level and a second level lower than the first level and the gate-on voltage continuously decreases from the first level to the second level for the predetermined time.

4. The liquid crystal display of claim 3, wherein

$$\frac{Von1+Vconst}{2}-\frac{Von1+Vconst}{2}\times 10\% \le Von2 \le \frac{Von1+Vconst}{2}+\frac{Von1+Vconst}{2}\times 10\%,$$

where Von1 and Von2 indicate the first and the second levels, respectively, and Vconst indicates a predetermined voltage level.

5. The liquid crystal display of claim 4, wherein the gray voltages include a plurality of pairs of a positive voltage (V^+) and a negative voltage (V^-) assigned to each gray and

$$\frac{V^+ + V^-}{2} = \text{Vconst for each gray.}$$

6. The liquid crystal display of claim 5, wherein the continuous decrease of the gate-on voltage from the first level to the second level is linear.

7. The liquid crystal display of claim 5, wherein the continuous decrease of the gate-on voltage from the first level to the second level is performed around a time when the gate signal moves from the gate-on voltage to the gate-off voltage.

8. The liquid crystal display of claim 7, wherein the gate-on voltage reaches the second level at a time when the gate signal moves from the gate-on voltage to the gate-off voltage.

9. The liquid crystal display of claim 1, further comprising a voltage generator including:

a first switch selectively transmitting a first voltage;

a first capacitor connected to the first switch and charging a voltage from the first switch; and

a second switch connected to the first capacitor and forming a discharging path of the voltage charged in the first capacitor.

10. The liquid crystal display of claim 9, wherein the voltage generator further comprises a resistor connected between the second switch and the first capacitor and the first switch discharges according to a time constant determined by a resistance of the resistor and a capacitance of the capacitor.

11. The liquid crystal display of claim 9, wherein the voltage generator further comprises:

a signal generator for generating a pulse signal with a predetermined period;

a voltage divider diving the first voltage; and

a second capacitor for charging a voltage from the voltage divider for turning on and turning off the first switch responsive to the pulse signal from the signal generator,

wherein the first switch and the second switch are alternately activated based on the pulse signal from the signal generator.

12. The liquid crystal display of claim 11, wherein the first switch comprises a PNP bipolar transistor and the second switch comprises an NPN bipolar transistor.

13. The liquid crystal display of claim 12, wherein the signal generator is connected to a base of the PNP bipolar transistor and is connected to a base of the NPN bipolar transistor via the first capacitor.

14. The liquid crystal display of claim 12, wherein the voltage divider comprises a first resistor and a second resistor connected in series between the first voltage and a ground and is connected to a base of the PNP generator, and

$$\frac{Vbe2}{Vn} \leq \frac{1}{1+(R2/R1)} < \frac{Vbe2+(Vhigh-Vlow)}{Vn},$$

where R1 and R2 are resistances of the first and the second resistors, respectively, Vbe2 is a base-emitter voltage of the PNP transistor, Vn is a value of the first voltage, and Vhigh and Vlow are high and low levels of the pulse signal of the signal controller, respectively.

15. A method of driving a liquid crystal display including a plurality of gate lines, a plurality of data lines, and a plurality of pixels including switching elements connected to the gate lines and the data lines, the method comprising:

generating a plurality of pairs of a positive gray voltage (V^+) and a negative gray voltage (V^-) for respective grays satisfying $\frac{V^+ + V^-}{2} = Vconst$, where Vconst is a predetermined value;

generating a gate signal including a gate-on voltage for turning on the switching element and a gate-off voltage for turning off the switching element;

applying the gate signal to the gate lines; and

applying the gray signals to the data lines,

wherein the gate-on voltage decreases from a first level (Von1) to a second level (Von2) for a predetermined time and

$$\frac{Von1+Vconst}{2} - \frac{Von1+Vconst}{2} \times 10\% \leq Von2 \leq \frac{Von1+Vconst}{2} + \frac{Von1+Vconst}{2} \times 10\%.$$